AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) An embedded disk controller having a servo controller, the embedded disk controller comprising:

a servo controller interface ~~that includes~~ including a speed matching module and a pipeline control module such that ~~at least two processors including~~ a first processor and a second ~~processors~~ processor share memory mapped registers without conflicts,

wherein the first processor and the second ~~processors~~ processor operate at different rates, and the ~~servo controller interface is~~ speed matching module and the pipeline control module are directly connected to the servo controller in between (i) the servo controller and (ii) the first processor and the second ~~processors~~processor.

2. (Currently Amended) The controller of Claim 1, ~~where~~ wherein the first processor operates at a first frequency, and the second processor operates at a second frequency.

3. (Currently Amended) The controller of Claim 1, ~~where~~ wherein the servo-controller and the servo controller interface operate in same or different frequency domains.

4. (Currently Amended) The controller of Claim 1, wherein the speed matching module ensures communication without inserting wait states in a servo controller interface clock domain for write access to the servo controller.

5. (Currently Amended) The controller of Claim 1, ~~where~~ wherein there are no read conflicts between the first processor and the second processor.

6. (Currently Amended) The controller of Claim 1, wherein the servo controller interface provides a hardware mechanism for indivisible register access to the first processor or the second processor.

7. (Currently Amended) The controller of Claim 6, ~~where~~ wherein the hardware mechanism includes a semaphore.

9-47. (Cancelled)

48. (Currently Amended) The controller of Claim 1, ~~where~~ wherein the pipeline control module resolves conflict between first and second processor transactions of the first and second processors, respectively.

49. (Currently Amended) The controller of Claim 1, ~~where~~ wherein the first processor and the second processor communicate with the servo controller via two separate buses.

50. (Currently Amended) The controller of Claim 1, ~~where~~ wherein if there is a write conflict between the first processor and the second processor, the pipeline control module holds write access to the second processor.

51. (Currently Amended) The controller of Claim 6, ~~where~~ wherein the hardware mechanism is a semaphore register.

52. (Currently Amended) A system for reading and writing data to a storage medium, the system comprising:

a first processor operating at a first rate;

a second processor operating at a second rate, the second rate being different from the first rate;

an embedded disk controller having a servo controller interface module,

wherein the servo controller interface module ~~that~~ includes a speed matching module and a pipeline control module ~~such that at least two processors including~~to permit the first processor and the second ~~processors~~ processor to share memory mapped registers without conflicts, and

wherein ~~the first and second processors operate at different rates, and~~ the ~~servo controller interface module is~~ speed matching module and the pipeline control module are directly connected to the servo controller in between (i) the servo controller and (ii) the first processor and the second ~~processors~~processor.

53. (Currently Amended) The system of Claim 52, ~~where~~ wherein the first processor operates at a first frequency, and the second processor operates at a second frequency.

54. (Currently Amended) The system of Claim 52, ~~where~~ wherein the servo-controller and the servo controller interface operate in same or different frequency domains.

55. (Currently Amended) The system of Claim 52, wherein the speed matching module ensures communication without inserting wait states in a servo controller interface clock domain for write access to the servo controller.

56. (Currently Amended) The system of Claim 52, ~~where~~ wherein there are no read conflicts between the first processor and the second processor.

57. (Currently Amended) The system of Claim 52, wherein the servo controller interface provides a hardware mechanism for indivisible register access to the first processor or the second processor.

58. (Currently Amended) The system of Claim 57, ~~where~~ wherein the hardware mechanism includes a semaphore.

59. (Currently Amended) The system of Claim 52, ~~where~~ wherein the pipeline control module resolves conflict between first and second processor transactions of the first and second processors.

60. (Currently Amended) The system of Claim 52, ~~where~~ wherein the first processor and the second processor communicate with the servo controller via two separate buses.

61. (Currently Amended) The controller system of Claim 52, ~~where~~ wherein if there is a write conflict between the first

processor and the second processor, the pipeline control module holds write access to the second processor.

62. (Currently Amended) The system of Claim 57, ~~where~~ wherein the hardware mechanism is a semaphore register.

63. (Currently Amended) A servo controller interface for a disk controller having a servo controller, the servo controller interface comprising:

a first interface for communicating with a first processor over a first bus at a first rate; and

a second interface for communicating with a second processor over a second bus at a second rate,

wherein,

the first rate differs from the second rate, the servo controller interface selectively grants one of the first and second processors access to a servo controller, ~~and~~

the servo controller interface is connected and positioned between the servo controller and the first and second processors,

the servo controller interface is directly connected to the servo controller and the first and second buses, and

the servo controller interface does not include the first and second buses and the first and second processors.

64. (Currently Amended) The servo controller interface of claim 63, wherein the first processor operates at a first frequency, and the second processor operates at a second frequency.

65. (Currently Amended) The servo controller interface of claim 63, further comprising a speed matching module that resolves conflicts between at least first and second clock domains.

66. (Currently Amended) The servo controller interface of claim 65, wherein the speed matching module transitions servo controller accesses from one of the first and second clock domains to the other of the first and second clock domains.

67. (Currently Amended) The servo controller interface of claim 63, wherein the first processor and the second ~~processors~~ processor share memory mapped registers within the servo controller.

68. (Currently Amended) The servo controller interface of claim 65, wherein the speed matching module does not insert wait states in a clock domain of the servo controller interface during write access to the servo controller.

69. (Currently Amended) The servo controller interface of claim 63, further comprising a pipeline control module that resolves transaction conflicts between the first processor and the second processor.

70. (Currently Amended) The servo controller interface of claim 63, wherein the servo controller interface delays a write access for one of the first and second processors during write conflicts between the first and second processors.

71. (Currently Amended) A servo controller interface for a disk controller, the servo controller interface comprising:

first interface means for communicating with a first processor over a first bus at a first rate; and

second interface means for communicating with a second processor over a second bus at a second rate,

wherein,

the first rate differs from the second rate,

the servo controller interface selectively grants one of the first and second processors access to a servo controller, ~~and~~

the servo controller interface is connected and positioned between the servo controller and the first and second processors,

the servo controller interface is directly connected to the servo controller and the first and second buses, and

the servo controller interface does not include the first and second buses and the first and second processors.

72. (Currently Amended) The servo controller interface of claim 71, wherein the first processor operates at a first frequency, and the second processor operates at a second frequency.

73. (Currently Amended) The servo controller interface of claim 71, further comprising speed matching means for resolving conflicts between at least first and second clock domains.

74. (Currently Amended) The servo controller interface of claim 73, wherein the speed matching means transitions servo

controller accesses from one of the first and second clock domains to the other of the first and second clock domains.

75. (Currently Amended) The servo controller interface of claim 71, wherein the first and second processors share memory mapped registers within the servo controller.

76. (Currently Amended) The servo controller interface of claim 73, wherein the speed matching module does not insert wait states in a clock domain of the servo controller interface during write access to the servo controller.

77. (Currently Amended) The servo controller interface of claim 71, further comprising pipeline control means for resolving transaction conflicts between the first processor and the second processor.

78. (Currently Amended) The servo controller interface of claim 71, wherein the servo controller interface delays a write access for one of the first and second processors during write conflicts between the first and second processors.

79. (Currently Amended) A method for operating a servo controller interface having a first interface and a second interface, the method comprising:

communicating with a first processor over a first bus at a first rate using the first interface;

communicating with a second processor over a second bus at a second rate using the second interface;

selectively granting one of the first and second processors access to a servo controller with the servo controller interface; and

connecting and positioning the servo controller interface between the servo controller and the first and second processors, wherein,

the first rate differs from the second rate,

the servo controller is directly connected to the servo controller and the first and second interfaces, and

the servo controller interface does not include the first and second buses and the first and second processors.

80. (Currently Amended) The servo method of claim 79, wherein the first processor operates at a first frequency, and the second processor operates at a second frequency.

81. (Currently Amended) The method of claim 79, further comprising resolving conflicts between at least first and second clock domains at a speed matching module.

82. (Currently Amended) The method of claim 81, further comprising transitioning servo controller accesses from one of the first and second clock domains to the other of the first and second clock domains at the speed matching module.

83. (Currently Amended) The method of claim 79, wherein the first and second processors share memory mapped registers within the servo controller.

84. (Currently Amended) The method of claim 79, further comprising resolving transaction conflicts between the first processor and the second processor at a pipeline control module.

85. (Currently Amended) The method of claim 79, further comprising delaying a write access for one of the first and second processors during write conflicts between the first and second processors.